AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0030] with the following rewritten paragraph:

-- [0030] With reference to Fig. 3 and with continuing reference to Figs. 1 and 2, to determine threshold voltage (V_T), means for applying electrical stimulus 32 applies a voltage V_{DS} across the drain D and source S (contacts 18 and 20, respectively) and applies a voltage V_{GS} across gate G and the source S (chuck 14 and contact 20, respectively). For the purpose of measuring threshold voltage V_T, V_{DS} and V_{GS} are derived from a common voltage source. Stated differently, for the purpose of measuring the threshold voltage V_T, one terminal of a DC voltage source is connected to the drain D and gate G (contact 18 and chuck 14, respectively) of transistor T and the other terminal is connected to ~~substrate~~ <u>source</u> S (contact 20). This DC voltage is then swept from a first voltage, e.g., 0 volts, toward a second voltage, e.g., 15 volts. During this sweep, measurement means 34 measures the swept DC voltage and the current (I_{DS}) flowing between drain D and source S (contacts 18 and 20, respectively) in response to the swept DC voltage. An exemplary curve 38 of the drain-to-source current (I_{DS}) versus the swept DC voltage, in this example referred to as the gate-to-source voltage (V_{GS}), is shown in Fig. 3. --

Please replace paragraph [0033] with the following rewritten paragraph:

-- [0033] With reference to Fig. 5 and with continuing reference to Figs. 1-4, to determine the interface trap density (D_{IT}) of semiconductor top layer 8, means for applying electrical stimulus 32 applies a reference voltage V_R to drain D and/or ~~gate G~~ <u>source S</u> (contacts 18 and 20, respectively), of transistor T and applies a gate voltage V_G to gate G (chuck 14) of transistor T. Subject to maintaining the voltage applied between gate G and drain D and/or source S, i.e., V_{GD} and/or V_{GS}, below the threshold voltage V_T of SOI wafer 4, V_G is swept from a first value toward a second value and reference voltage V_R is changed to maintain transistor T below its threshold voltage V_T. During the sweep of V_G, measurement means 34 measures the total current flowing through the drain D and/or source S. Hereinafter, this total current is referred to as "I_D". Measurement means 34 then determines the base 10 logarithm ($\log_{10}$) of I_D at various points along the sweep of V_G and forms curve 44 of $\log_{10} I_D$ versus V_G. The trap density of the interface between semiconductor top layer 8 and buried oxide layer 6 is then simply the slope of curve 44. --

Please replace paragraph [0036] with the following rewritten paragraph:

-- [0036] Once drain conductance g_D and C_{OX} have been determined, the values determined therefor can be utilized in the following equation EQ2 to determine the carrier mobility (~~N~~ $\underline{\mu}$) of semiconductor top layer 8:

EQ2: $$\mu \approx Lg_D/[ZC_{OX}(V_{GS} - V_T)]$$

where: L = length of channel 36;

Z = the width of channel 36;

V_{GS} = the gate G to source S voltage applied to determine C_{OX}; and

V_T = threshold voltage determined in the manner discussed above in connection with Fig. 3. --

Please replace paragraph [0037] with the following rewritten paragraph:

-- [0037] A dopant concentration, or dopant density, of semiconductor top layer 8 can be determined from a doping profile of semiconductor top layer 8 determined by plotting threshold voltage V_T versus $(2\phi_F - V_{BS})^{1/2}$ and measuring a slope $m = \Delta V_T/\Delta\ (2\phi_F - V_{BS})^{1/2}$ where ϕ_F is ~~to~~ equal <u>to</u> the Fermi level of semiconductor top layer 8 and V_{BS} is equal to the voltage between semiconductor top layer 8 and source S (contact 20). --

Please replace paragraph [0039] with the following rewritten paragraph:

-- [0039] The doping concentration (N_{TOP}) of semiconductor top layer 8 can then be determined utilizing the following equation EQ3:

EQ3: $$N_{TOP} = m^2 C_{OX}^2/2qk_S\epsilon_0$$

where: m = doping profile of semiconductor top layer 8 determined in the manner described above;

C_{OX} is the capacitance of buried oxide layer 6 determined in the manner described above in connection with Fig. 6;

q = ~~equals~~ the charge of an electron;

k_S is the conduction factor of silicon determined in the manner described above in connection with Fig. 4; and

ϵ_0 is the permittivity of air. --